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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,074	07/15/2003	John Lam	174/273	1235

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,074	LAM ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-26* is/are allowed.

6)☒ Claim(s) *1,2,5-7,11,27,28,30,33 and 35-38* is/are rejected.

7)☒ Claim(s) *3,4,8-10,12,29,31,32 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/621,074 filed on 07/15/2003. Claims 1 – 38 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 27, line 4, after "circuitry;" insert —**and**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 2, 5 – 7, 27, 30, 33 and 35 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,652,529 to *Gould et al.* in view of U.S. Patent 4,059,842 to *Meacham*.

5. As to Claim 1, *Gould et al.* show and teach the following subject matter:

- Programmable logic arrays having programmable clock/reset resource – [title; abstract; col. 2, line 10 – 26];

- A signal distributing architecture (i.e., network) for clock and reset signal distribution in a programmable array ... networks for distributing clock and *reset signals* to logic cells of the (programmable logic) array – [abstract; Fig. 4]; Notice that, due to configurable capabilities of the programmable logic array, the *logic cells in the programmable logic array* can be constructed to form an intellectual property block that has a plurality of channels and support a multi-channel input/output protocol;
- *Reset distribution network* (i.e., circuitry) – [col. 2, line 30 – 38]; routing reset signals from *reset signal source* to the logic cells – [col. 2, line 10 – 26]; Notice that a reset signal is routed to each of the plurality of channels formed by the logic cells;
- *Reset distribution network/circuitry* is designed to be *low skew* – [col. 3, line 66 – col. 4, line 5]; It means that the *reset distribution network/circuitry* is operative to be skew-tolerant.

Gould et al. do not show and teach routing the reset signal through a plurality of channels during a same clock cycle and wherein the reset signal is glitch-free. But *Meacham* teaches a method of using a synchronizer and a combinatorial circuit to form an *phase synchronization reset signal* having a period equal one-half the period of the cycle of the master clock – [col. 4, line 44 – 63; Fig. 3; Fig. 4]. Notice that the purpose of generating phase *synchronization reset signal* is to achieve a glitch-free reset signal.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Meacham* in utilizing a synchronizer and a combination circuit in the reset distribution network/circuitry to generate *phase synchronization reset signal* having a period equal one-half the period of the cycle of the master clock in order to achieve a glitch-free reset signal to be distributed through a plurality of channels in the intellectual property block.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 27, reasons are included in **[Response A]** given above.

7. As to Claim 35, in addition to programmable logic resource as recited in **[Response A]** given above, a digital processing system comprises processing circuitry and a memory (e.g., RAM) coupled to the processing circuitry.

8. As to Claims 36 – 38, reasons are included in **[Response A]** given above. Notice that a programmable logic resource as defined in Claim 27 can be mounted on a printed circuit board. A memory and processing circuitry can be mounted on the same printed circuit board; the memory is coupled to the programmable logic resource, and the processing circuitry is coupled to the programming logic resource.

9. As to Claims 2 and 30, *Meacham* shows in Fig. 3 a circuitry comprises flip-flops 30, 32, and combinatorial logic 34, 36 that receives as input a reset signal at pin 26 and output a phase synchronized reset signal at output of gate 36. Notice that the phase synchronized reset signal at output of gate 36 can be routed to each of the plurality of channels via reset signal distribution network/circuitry.

10. As to Claims 5 – 7, in addition to reasons included in **[Response A]** given above, *Meacham* shows the subject matter in Fig. 3 and Fig. 4. Notice that (1) the synchronizer is made of a first flip-flop 30 and a second flip-flop 32 as indicated in Fig. 3 (2) logic circuitry, that is made of gates 34 and 36, receives as input the output from the synchronizer and generates as output a single reset signal.

For reference purposes, the explanations given above in response to Claims 5 – 7 are called **[Response B]** hereinafter.

11. As to Claim 33, reasons are included in **[Response B]** given above.

12. Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,652,529 to *Gould et al.* and U.S. Patent 4,059,842 to *Meacham* in view of U.S. Patent 4,983,857 to *Steele*.

13. As to Claim 11, *Gould et al.* and *Meacham* show and teach all subject matter recited in Claim 1, they do not teach subject matter regarding a control logic that

receives as inputs the reset signal, a first signal, and a second signal each generated from the programmable logic resource core circuitry, wherein the first signal and the second signal control when the reset signal is output from the control logic and sent as input to the (reset distribution) circuitry. But *Steele* discloses using a controller (i.e., control logic) in a programmable logic device and applying information regarding a *predetermined minimum level of the supply voltage* (i.e., a *first signal*) for all parts on the chip and *when all parts of the chips have reached a stable operating voltage* (i.e., a *second signal*) to *control power-up reset circuitry* – [title; abstract; col. 1, line 10 – 38].

Notice that the first signal and the second signal are applied by the control logic in order to ensure that, when performing power-up reset on a plurality channels in an intellectual property block, the reset signal is delayed until circuits of all channels have reached their respective stable operating voltage.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Steele* in applying information regarding a *predetermined minimum level of the supply voltage* (a *first signal*) for all circuits of a plurality channels in an intellectual property block and *when all the plurality of channels have reached a stable operating voltage* (a *second signal*) to *control power-up reset circuitry* (i.e., logic) in order to ensure that, when performing power-up reset, the reset signal is delayed until circuits all channels have reached their respective *stable operating voltage*.

For reference purposes, the explanations given above in response to Claim 11 are called **[Response C]** hereinafter.

14. As to Claim 28, reasons are included in **[Response C]** given above.

Allowable Subject Matter

15. Claims 13 – 26 are allowed. Claims 3, 4, 8 – 10, 12, 29, 31, 32 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- The programmable logic resource of Claim 2 wherein each of a plurality of reset signals comprises a *receiver reset signal* in combination with other limitations as recited in **Claim 3** and **Claim 31**, respectively;
- The programmable logic resource of Claim 2 wherein each of a plurality of reset signals comprises a *transmitter reset signal* in combination with other limitations as recited in **Claim 4** and **Claim 32**, respectively;
- The programmable logic resource of Claim 7 wherein a logic circuitry comprises an OR gate in combination with other limitations as recited in **Claim 8**;
- The programmable logic resource of Claim 7 wherein the (reset distribution) circuitry comprises a *secondary synchronizer* in each of the plurality of channels in combination with other limitations as recited in **Claim 9**;
- The programmable logic resource of Claim 11 wherein the second signal indicated when programming of configuration data on the programmable logic resource core circuitry is completed in combination with other limitations as recited in **Claim 12** and **Claim 29**, respectively;
- A programmable logic resource having programmable logic resources core circuitry that provides a reset signal to an intellectual property block having a plurality of channels comprises second circuitry in each of the plurality of channels that is coupled to a central block and is operative to further synchronize a single reset signal, which is first synchronized by and outputted from first circuitry in the central block, for output in each of the plurality of channels in combination with other limitations as recited in **independent Claim 13**;
- The programmable logic resource of Claim 34 wherein the reset circuitry further comprises a second set of synchronizers in combination with other limitations as recited in **Claim 34**;

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
July 21, 2005